IN THE CLAIMS:

Please enter the following claim set:

1-47. (canceled)

48. (previously amended) A method of fabricating a semiconductor device comprising:

forming a pad;

forming a protective insulating region on the pad including first and second insulating layers, the first insulating layer being in direct contact with the pad and the second insulating layer being in direct contact with the first insulation layer; the second insulating layer comprising silicon nitride;

forming a mask layer on the protective insulating region in direct contact with a surface of the second insulating layer, the second insulating layer being positioned between the first insulating layer and the mask layer, the mask layer including an aperture in a region corresponding to an electric connection region of the pad; and

dry etching through the surface of the second insulating layer at the aperture in the mask to form an opening extending through the second insulating layer and the first insulating layer to the pad, wherein an etchant gas comprising CF_4 and O_2 is used to form the opening extending through the second insulation layer, and wherein at least a portion of the opening has a tapered shape.

49. (previously amended) A method as in claim 48, wherein the dry etching comprises isotropically etching at least a portion of the second insulating layer and anisotropically etching at least a portion of the first insulating layer.

50-51. (canceled)

52. (previously amended) A method as in claim 48, wherein at least a side surface of the second insulating layer surrounding the electric connection region has a tapered surface with an acute angle to the top surface of the pad after the dry etching.

53. (previously amended) A method as in claim 48, wherein an angle of the side surface of the second insulating layer surrounding the opening is smaller than a tapered angle of a side surface of the first insulating layer surrounding the opening.

54. (previously amended) A method as in claim 48, wherein an angle between a side surface of the second insulating layer surrounding the opening and a top surface of the pad is in the range of 30° to 60°.

55. (previously amended) A method as in claim 54, wherein an angle between a side surface of a portion of the first insulation layer surrounding the opening and the top surface of the pad is in the range of 60° to 90°.

56. (previously amended) A method as in claim 48, wherein a distance between an upper end of a side surface of the first insulating layer surrounding the opening and a lower end of the side surface of the second insulating layer surrounding the opening is in the range of 0 μm to 3 μm.

57. (previously added) A method as in claim 56, wherein the distance is in the range of 0 μm to 1 μm.

58. (previously amended) A method as in claim 48, wherein an aperture formed in the second insulating layer after the dry etching is larger than an aperture formed in the first insulating layer after the dry etching.

59. (previously added) A method as in claim 48, comprising forming a bump electrode on the electric connection region in the pad through a barrier layer.

60. (previously added) A method as in claim 48, comprising forming the first insulating layer from a material comprising silicon oxide.

61. (currently amended) A method as in claim 60, wherein ~~the same~~ an etchant gas comprising CF_4 is used to etch the first insulating layer and an etchant gas comprising CF_4 is used to etch the second insulating layer.

62. (previously amended) A method as in claim 61, wherein the first insulating layer and the second insulating layer are etched in a continuous manner.

63. (previously amended) A method as in claim 48, wherein the first insulating layer and the second insulating layer are etched in a continuous manner.

64. (previously amended) A method for forming a bonding pad area using a dry etch process, comprising:

forming a conducting pad in electrical contact with an electronic device;

forming a protective insulation layer on a surface of the conducting pad, the protective insulation layer including at least first and second insulating layers, wherein the first insulating layer and the second insulating layer are formed from materials having different compositions, the first insulating layer comprising a silicon oxide layer, the second insulating layer comprising a silicon nitride layer, the silicon oxide layer being formed on the conducting pad, the silicon nitride layer being formed on the silicon oxide layer;

forming a mask in direct contact with a surface of the protective insulation layer and providing an opening in the mask; and

dry etching through the surface of the protective insulation layer at the opening in the mask to form an aperture extending through the silicon nitride layer and the silicon oxide layer to

the surface of the pad using CF_4 and O_2 as an etchant, so that the silicon nitride layer includes a side surface surrounding the aperture, the silicon nitride layer side surface having a tapered shape with an angle in the range of 30 degrees to 60 degrees in relation to the surface of the conducting pad, and the silicon oxide layer includes a side surface surrounding the aperture, the silicon oxide layer side surface having a tapered shape with an angle in the range of 60 degrees to 90 degrees in relation to the surface of the conducting pad.

65. (previously amended) A method as in claim 64, wherein the protective insulation layer consists of the first insulating layer and the second insulating layer, the first insulating layer consisting of a silicon oxide layer and the second insulating layer consisting of a silicon nitride layer.

66. (previously amended) A method as in claim 65, wherein the dry etching includes continuously etching the second insulating layer and the first insulating layer.

67. (previously amended) A method as in claim 64, wherein the dry etching includes isotropic etching of at least part of the silicon nitride layer and anisotropic etching of at least part of the silicon oxide layer.

68. (currently amended) A method of fabricating a semiconductor device comprising:

forming a pad with a predetermined pattern on an insulating layer;

forming a protective insulating layer on a surface of the pad;

forming a mask layer in direct contact with a surface of the protective insulating layer, the mask layer having an aperture in a region corresponding to an electrical connection region of the pad; and

dry etching through the protective insulating layer using an etchant comprising CF_4 ~~and O_2~~ to form an opening extending through the protective insulating layer to the electrical connection region of the pad, so that the protective insulating layer includes a side surface

surrounding the opening, the side surface being tapered so that the opening of the protective insulation layer at the pad surface is smaller than the opening of the protective insulation layer a distance away from the pad surface.

69. (previously added) A method as in claim 68, wherein wherein the protective insulating layer has a thickness of 1000 nm to 2000 nm.

70. (previously amended) The method of fabricating a semiconductor device of claim 68, wherein a tapered angle between the side surface of the insulating layer surrounding the opening is in the range of 10° to 80°.

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71. (previously added) The method of fabricating a semiconductor device of claim 68, wherein a bump electrode is provided on the electric connection region of the pad through a barrier layer.

72. (previously amended) The method of fabricating a semiconductor device of claim 68, wherein the protective insulating layer is formed from one of a silicon oxide layer and a silicon nitride layer.

73. (previously added) The method of fabricating a semiconductor device of claim 68, wherein the protective insulating layer is formed from a silicon oxide layer and a silicon nitride layer, the silicon oxide layer being formed above the pad and the silicon nitride layer formed above the silicon oxide layer.

74. (currently amended) The method of fabricating a semiconductor device of claim 73, wherein the ~~etchant consists of CF_4 and O_2 and the~~ etching is carried out continuously.

75. (new) The method of fabricating a semiconductor device of claim 68, wherein the protective insulating layer consists of single layer of silicon nitride.

76. (new) The method as in claim 48, wherein an angle between a side surface of the second insulating layer surrounding the opening and a top surface of the pad is in the range of 30° to 40°.

77. (new) A method as in claim 76, wherein an angle between a side surface of a portion of the first insulation layer surrounding the opening and the top surface of the pad is in the range of 60° to 70°.

78. (new) A method of fabricating a semiconductor device comprising:

forming a pad with a predetermined pattern on an insulating layer;

forming a protective insulating layer on a surface of the pad;

forming a mask layer in direct contact with a surface of the protective insulating layer, the mask layer having an aperture in a region corresponding to an electrical connection region of the pad;

dry etching through the protective insulating layer to form an opening extending through the protective insulating layer to the electrical connection region of the pad, so that the protective insulating layer includes a side surface surrounding the opening, the side surface being tapered so that the opening at the pad surface is smaller than the opening a distance away from the pad surface;

after the dry etching, removing the mask layer; and

after removing the mask layer, heating the device at a temperature in the range of 350°C - 450°C.

79. (new) A method as in claim 78, wherein the protective insulation layer comprises a silicon oxide layer and a silicon nitride layer, wherein the silicon oxide layer includes a side surface having a different angle with respect to an upper surface of the pad than the silicon nitride layer.

80. (new) A method as in claim 79, wherein both the side surface of the silicon oxide layer and the side surface of the silicon nitride layer are tapered to that a lower portion defines an opening region that is smaller than that defined by an upper portion.

81. (new) A method as in claim 78, wherein the silicon oxide includes a side surface having an angle with respect to an upper surface of the pad that is in the range of 60 to 70 degrees.

82. (new) A method as in claim 81, wherein the silicon nitride includes a side surface having an angle with respect to an upper surface of the pad that is in the range of 30 to 40 degrees.

83. (new) A method of fabricating a semiconductor device comprising:

forming a pad;

forming a protective insulating region on the pad comprising first and second insulating layers, the first insulating layer being in direct contact with the pad and the second insulating layer being in direct contact with the first insulation layer; the second insulating layer comprising silicon nitride;

forming a mask layer on the protective insulating region in direct contact with a surface of the second insulating layer, the second insulating layer being positioned between the first insulating layer and the mask layer, the mask layer including an aperture in a region corresponding to an electric connection region of the pad; and

dry etching through the surface of the second insulating layer at the aperture in the mask to form an opening extending through the second insulating layer and the first insulating layer to the pad,

wherein the dry etching includes (1) etching the second insulation layer to define a tapered shape so that the opening extending through the protective insulation layer gets progressively smaller from an upper portion of the second insulation layer to a lower portion of the second insulating layer, and (2) etching the first insulation layer to define a tapered shape so

that the opening extending through the first insulation layer gets progressively smaller from an upper portion of the first insulation layer to a lower portion of the second insulation layer,

and wherein the dry etching is controlled so that the first insulation layer includes an upper surface portion exposed to the opening, the upper surface portion extending between an upper end of a side surface of the first insulation layer and a lower end of a side surface of the second insulation layer, wherein the side surface of the first insulation layer and the side surface of the second insulation layer are both exposed to the opening.

84. (new) A method as in claim 83, wherein the etching is controlled so that the upper surface portion exposed to the opening extends a distance of up to 3 nm between the upper end of the side surface of the first insulation layer and the lower end surface of the second insulation layer.

85. (new) A method as in claim 83, wherein the etching is controlled so that the upper surface portion of the fist insulation layer is substantially parallel to an upper surface of the pad.

86. (new) A method as in claim 83, further comprising:

forming a barrier layer in the in the opening, the barrier layer being positioned on: (1) the side surface of the first insulation layer exposed to the opening, (2) the upper surface portion of the first insulation layer exposed to the opening; and (3) the side surface of the second insulation layer exposed to the opening; and

forming a bump electrode on the barrier layer in the opening.

87. (new) A method as in claim 83, wherein the etching is controlled so that the side surface of the first insulation layer includes an angle in the range of 60 - 70 degrees with respect to an upper surface of the pad, and the side surface of the second insulation layer includes an angle in the range of 30 - 60 degrees with respect to the upper surface of the pad.

88. (new) A method as in claim 83, further comprising removing the mask layer after the etching and then heating the device at a temperature of 350°C to 450°C.

89. (new) A method as in claim 88, wherein the device is heated at 350°C to 450°C for a time of 10 to 20 minutes.

90. (new) A method as in claim 83, further comprising forming a polyimide resin layer on the second insulation layer.